Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **4**
2. **2**
3. **0**
4. **7**
5. **9**
6. **5**
7. **6**
8. **VSS**
9. **8**
10. **A**
11. **D**
12. **C**
13. **B**
14. **1**
15. **3**
16. **VDD**

**.068”**

**.070”**

**2 1 16**

**MASK**

**REF**

**15**

**14**

**13**

**12**

**11**

**3**

**4**

**5**

**6**

**7 8 9 10**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VDD**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .068” X .070” DATE: 11/9/17**

**MFG: TEXAS INSTR. / HARRIS THICKNESS .011” P/N: CD4028BH**

**DG 10.1.2**

#### Rev B, 7/19/02